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10/618,060	07/11/2003	Robert Jackson	15114H-068300US	4329

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EXAMINER	
DINH, PAUL	
ART UNIT	**PAPER NUMBER**
2825	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/11/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/618,060	JACKSON, ROBERT	
	Examiner	Art Unit	
	Paul Dinh	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 March 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *16-28 and 31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *16-28 and 31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This FINAL office action is a response to the amendment and remarks filed on 3/23/07.

The rejections based on Vorbach, Brewer, and Gemelli are maintained.

Claims 16-28 and 31 are pending.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form The basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) The invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) The invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. Claims 16-27 and 31 are rejected under 35 U.S.C. 102(e) as being anticipated by the prior art of record Gemelli (US Pub. 2003/0101307)

(Claim 16)

Receive a system design including component connected via component ports from a system designer

(One or more of fig 9, 12-13, 15-16, 29 and corresponding text, i.e., abstract, para 0002-0003, 0016, 0018, 0025-0026, 0042, 0044, 0051-0052, 0056-0057, 0061-0062, etc; component is one or more of: peripheral modules, macro-cells, memories, microprocessor, ASIC, FPGA, FIFO, pre-verified design elements that connected as "virtual component " build the system; devices connected by bus, user developed components, etc, these components connected via component port from a system designer/developer);

For each of the component ports, identifying a set of alternative bus/communication protocols supported by the component port

(One or more of fig 9, 12-13, 15-17, 29 and corresponding text, i.e.

Para 0018: "To make possible communication between microprocessor and Developed components those components need a microprocessor interface. The Microprocessor interface is generally build as a macro-cell and embedded in one Of the user developed components);

Para 0084: main purpose of the invention is that to indicate an interface bus protocol able to manage in a transparent way the round-trip latency of communication between microprocessor and resources:

Para 0094 "the development of an efficient interface bus protocol, as it will be seen

Para 0164: the COMMON-BUS highly reduces the number of interconnections between DMI Peripherals

Para 0501: "Now a protocol governing transactions through the COMMON-BUS is Disclosed. This protocol will be named COMMON BUS PROTOCOL"; etc)

Comparing the sets of alternative bus/communication protocols of the component ports to identify a subset of the sets of alternative bus/communication protocols supported by all of the component ports; and

(One or more of fig 9, 12-13, 15-16, 29 and corresponding text)

Selecting one of the subset of the bus/communication protocols to implement connections between the components via the component ports

(I.e., common bus protocol, common information carried by the REGISTER-COMMON-BUS (para 0221); width of common bus (claim 5); status word of common bus (claim 32); peripheral selection, interface bus protocol selection, ports selection in para 0001 0094-0095, 0099, 0170, 0171, 0179-0180, 0203-0205, 0207-0212, 0308, 0367, 0374, 0503, 0505, 0652, 0771, claim 1, etc).

(Claims 17-18, 20) wherein comparing the sets of alternative bus/communication protocols comprises comparing a parameter value/operation/connection values of a first one of the set of alternative bus/communication protocols supported by a first one of the component ports with corresponding parameter values/operation/connection values of each of the sets of alternative bus/communication protocols supported by the other component ports to identify the subset of the bus/communication protocols having compatible parameter values/operations/connection values (one or more of fig 2, 12-13, 15-17, 29, 31-38, 40-43; operation = i.e., one or more of master, slave, idle read, write, DMI, DMA, mode, priority, , system execution, etc)

(Claim 19) wherein the subset of the bus/communication protocols having a compatible operation includes a first operation (i.e., read/write and/or master/slave and/or idle/execution) associated with a first one of the component ports and a complementary operation (i.e.,

write/read and/or slave/master and/or execution/idle) associated with at least one of the other component ports.

(Claim 21) wherein the subset of the bus/communication protocols having compatible connection values includes an input for a first operation associated with first one of the component ports and an output for the first operation associated with at least one of the other component ports (one or more of: fig 2, 12-13, 15-17, 29, 31-38, 40-43).

(Claim 22) wherein comparing the sets of alternative bus/communication protocols comprises comparing a role value of a first one of the set of alternative bus/communication protocols supported by a first one of the component ports with corresponding role values of each of the sets of alternative bus/communication protocols supported by the other component ports to identify the subset of the bus/communication protocols having compatible role values (one or more of: fig 2, 12-13, 15-17, 29, 31-38, 40-43; operation = i= i.e., one or more of master, slave, idle read, write, DMI, DMA, mode, priority, , system execution, etc); wherein each role values is associated with at least one operation, wherein each connection value is associated with at least one operation, wherein each operation is associated with at least one parameter value (one or more of: fig 2, 12-13, 15-17, 29, 31-38, 40-43)

(Claim 23) wherein selecting one of the subset of the bus/communication protocols to implement connections between the components via the component ports comprises determining the number of bus/communication protocols included in the subset (one or more of: fig 2, 12-13, 15-17, 29, 31-38, 40-43); in response to the subset having a single bus/communication protocol, selecting the single bus/communication protocol (one or more of: fig 2, 12-13, 15-17, 29, 31-38, 40-43); in response to the subset being an empty set, notifying the designer that the connections between the components via the component ports can not be made (one or more of: fig 2, 12-13, 15-17, 29, 31-38, 40-43).

(Claims 24-25) in response to the subset including at least two bus/communication protocols, automatically selecting one of the subset of the bus/communication protocols to implement connections between the components via the component ports (one or more of: fig 2, 12-13, 15-17, 29, 31-38, 40-43); presenting the subset to the system designer (one or more of: fig 2, 12-13, 15-17, 29, 31-38, 40-43)

(Claims 26-27) wherein identifying a set of alternative bus/communication protocols supported by the component port comprises: for each component port, retrieving corresponding component information from a component library wherein the component library is stored in a database (0475)

(Claim 31) analyzing the selected on of the subset of bus/communication protocols to identify a first set of connection defined by the selected one of the subset of bus/communication protocols (one or more of: fig 2, 12-13, 15-17, 29, 31-38, 40-43); analyzing the component ports of the components to identify the connections used by the component ports for the selected one of the subset of bus/communication protocols (one or more of: fig 2, 12-13, 15-17, 29, 31-38, 40-43); and comparing the connection used by the component port of the components with the first set of connections to determine a portion of the first set of connection necessary to implement the connections (one or more of: fig 2, 12-13, 15-17, 29, 31-38, 40-43)

2. Claims 16-27 are rejected under 35 U.S.C. 102(b) as being anticipated by the prior art of record Vorbach (USP 6721830)

(Claim 16) Receive a system design including component connected via component ports from a system designer (abstract, fig 9-16 and corresponding text, component = one or more of: cells, units, memory, peripheral, FPGA, etc);

For each of the component ports, identifying a set of alternative bus/communication protocols supported by the component port

(Abstract, fig 9-16 and corresponding text, i.e.:

Col 3; "obtain appropriate bus architectures, a plurality of internal lines are combined in buses where n denotes the number of the bus, bus system/values in fig 10-16;);

Comparing the sets of alternative bus/communication protocols of the component ports to identify a subset of the sets of alternative bus/communication protocols supported by all of the component ports (abstract, fig 10-16 and corresponding text); and

Selecting one of the subset of the bus/communication protocols to implement connections between the components via the component ports (abstract, fig 10-16)

(Claims 17-18, 20) wherein comparing the sets of alternative bus/communication protocols comprises comparing a parameter value/operation/connection values of a first one

of the set of alternative bus/communication protocols supported by a first one of the component ports with corresponding parameter values/operation/connection values of each of the sets of alternative bus/communication protocols supported by the other component ports to identify the subset of the bus/communication protocols having compatible parameter values/operations/connection values (fig 10-16)

(Claim 21) wherein the subset of the bus/communication protocols having compatible connection values includes an input for a first operation associated with first one of the component ports and an output for the first operation associated with at least one of the other component ports (fig 6-9)

(Claim 23) wherein selecting one of the subset of the bus/communication protocols to implement connections between the components via the component ports comprises determining the number of bus/communication protocols included in the subset (fig 10-16); in response to the subset having a single bus/communication protocol, selecting the single bus/communication protocol (fig 12); in response to the subset being an empty set, notifying the designer that the connections between the components via the component ports can not be made (fig 12-16)

(Claims 24-25) in response to the subset including at least two bus/communication protocols, automatically selecting one of the subset of the bus/communication protocols to implement connections between the components via the component ports (fig 13-16); presenting the subset to the system designer (fig 13-16)

(Claims 26-27) wherein identifying a set of alternative bus/communication protocols supported by the component port comprises: for each component port, retrieving corresponding component information from a component library wherein the component library is stored in a database (fig 12)

(Claims 29-30) wherein at least one of the connections is between to components component within a PLD (fig 10, 12); wherein at least one of the connections is between a components component within a first PLD and a component external to the first PLD (fig 10, 12)

3. Claim 16 is rejected under 35 U.S.C. 102(e) as being anticipated by the prior art of record Brewer (USP 6895477)

(Claim 16) Receive a system design including component connected via component ports from a system designer (fig 1-2);

For each of the component ports, identifying a set of alternative bus/communication protocols supported by the component port (fig 2, a set of alternative bus/communication = universal bus (abstract) and/or bus protocol selected by bus selector);

Comparing the sets of alternative bus/communication protocols of the component ports to identify a subset of the sets of alternative bus/communication protocols supported by all of the component ports (summary, fig 1-2); and

Selecting one of the subset of the bus/communication protocols to implement connections between the components via the component ports (abstract, summary, fig 2)

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a), which forms the basis for all obviousness rejections, set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 28 is rejected under 35 U.S.C. 103(a) as being unpatentable over one or more of: Vorbach (USP 6721830) and Gemelli (US Pub. 2003/0101307) in view of one or more of Beunings (US pub. 2003/0217176), Bales (US pub. 2004/0068554)

Vorbach and Gemelli disclose substantially all the elements in claim 28 except XML.

Beunings discloses XML in para 0017.

Bales discloses XML in para 0035.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use XML simply because one or more of the followings:

XML is known in the art for communication protocol (by Bales in para 0035).

XML is a communication protocol standard (by Beunings in para 0017).

Response to Applicant Remarks

Even though the Applicant fails to address three references, Vorbach, Brewer, and Gemelli, applied in the non-final rejection; the examiner, after reconsidering the claims and the references, finds that the references disclose all the elements in the claims as detailed above.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul Dinh whose telephone number is 571-272-1890. If attempts to reach the examiner by telephone are unsuccessful, the examiner's Supervisor, Jack Chiang can be reached on 571-272-7483. The fax number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Paul Dinh
Primary Examiner